

## **AMENDMENTS TO THE CLAIMS:**

1. (currently amended) A method of forming a DRAM cell array comprising the steps of:

(a) forming a plurality of deep trenches in an array portion of a Si-containing substrate having at least a hard mask formed thereon, said plurality of deep trenches being arranged in rows and columns and including at least collar oxide regions formed on sidewalls of the deep trenches thereof and a recessed deep trench conductors formed in the deep trenches ~~between said collar oxide regions~~ and defining a capacitor electrodes for a DRAM cell;

(b) forming a buried-strap outdiffusion regions within a portions of said sidewalls ~~such that said portion partially encircles said wall;~~

(c) forming a nitride liner layer above a horizontal surfaces of said deep trench conductors and enclosing exposed sidewalls and collar oxide regions;

(d) depositing a top trench oxide (TTO) layer above said formed nitride liner layer;

(e) performing a TTO sidewall etch to remove TTO oxide which has been deposited on the vertical sidewalls and collar oxide regions, said nitride liner acting to protect said collar oxide regions ~~layer~~ from being etched;

(f) performing a nitride liner etch to remove ~~the portions~~ of the TTO nitride liner which is ~~are~~ exposed after TTO oxide removal;

(g) forming a vertical MOSFET by growing a gate dielectric on exposed sidewalls of said deep trenches and forming a gate conductors above said TTO oxide layer within the sidewalls of the deep trenches lined with said gate dielectric, wherein said formed TTO

layer having an underlying nitride liner eliminates possibility of TTO dielectric breakdown between said gate conductorsg and said capacitor electrodesg of a DRAM cell.

2. (currently amended) The method of Claim 1, wherein prior to said step (c), the step of depositing a sacrificial oxide layer above ~~a~~ horizontal surfacesg of said deep trench conductorsg and ~~surrounding over~~ exposed sidewallsg and collar oxide regions.

3. (currently amended) The method of Claim 1, wherein said nitride liner etch of step f) is ~~selective to~~ stops at and does not etch the oxide and silicon.

4. (currently amended) The method of Claim 2, wherein said nitride liner etch of step f) stops at and does not etch ~~is selective to~~ said sacrificial oxide layer ~~when said sacrificial oxide layer is grown under the nitride liner.~~

5. (original) The method of Claim 1, wherein said collar oxide regions are formed by a local oxidation of silicon process.

6. (currently amended) The method of Claim 5, wherein prior to forming said collar oxide regions ~~a capacitors~~are ~~is~~ formed in a bottom portionsg of said deep trenches.

7. (currently amended) The method of Claim 6, wherein said capacitors are ~~is~~ formed by the steps of: forming a buried plate diffusion regionsg about said deep trenches, lining walls of said deep trenches with a node dielectric and filling said deep trenches with said deep trench conductorsg.

8. (currently amended) The method of Claim 6, wherein said recessed deep trench conductorsare ~~is~~ formed by deposition of a deep trench conductorsg and etching.

9. (currently amended) The method of Claim 1, wherein said buried-strap outdiffusion regions are ~~is~~ formed by a one-sided strap process.

10. (currently amended) The method of Claim 9, wherein said one-sided strap process includes forming said ~~a divot filled~~ collar oxide regions.